PATENT

Attorney Docket No.: BEA9-2000-0013-US1

BOARD OF PATENT APPEALS
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	McKenney et al.		
SERIAL NO.:	09/753,062	Group Art Unit:	2112
FILING DATE:	December 28, 2000	Examiner:	Huynh, K.
FOR:	**Quad Aware Locking Primitive**		

BRIEF OF PATENT OWNER ON APPEAL

1. Real Party in Interest

International Business Machines Corporation, a New York corporation, is the real party in interest.

2. Related Appeals and Interferences

There are no related appeals or interferences.

3. Status of Claims

Claims 1-31 remain pending in the application. The claims on Appeal are included in the Appendix.

4. ***Status of Amendments***

No amendments to claims have been submitted.

5. ***Summary of Claimed Subject Matter***

Applicants' invention includes a computer system with a plurality of processors organized into a hierarchy with instructions to enable a lock to be passed to a waiting processor on an intra-quad basis when appropriate, and passed to a waiting processor on an inter-quad basis when a particular quad has been monopolizing the lock for an extended prior of time. This hierarchical ranking of the processors together with processing the lock responsive to the hierarchy enables equitable access to and distribution of the lock in a heavy contention environment and thereby increases the efficiency of the system. Accordingly, the hierarchical design of the processors together with the processing of the lock responsive to the hierarchy enables the processors to achieve increased performance at both low and high levels of contention.

With respect to claim 1, support for the elements in line 2 of the body of the claim is found in the original specification on page 1, lines 5-6, page 4, lines 3-5, and page 26, lines 31-32, support for the elements in lines 2 and 3 of the body of the claim is found in the original specification on page 11, lines 6-25, and page 27, lines 8-10, support for the elements in line 4 of the body of the claim is found in the original specification on page 1, lines 6-7, and page 4, lines 3-5.

With respect to claim 13, support for the elements in line 1 of the body of the claim is found on page 5, lines 24-26, support for the elements found on lines 2-3 of the body of the claim is found on page 11, lines 6-25 and page 27, lines 8-10, support for the elements found in line 4 of the body of the claim is found on page 1, lines 5-6, page 4, lines 3-5, and page 26, lines 31-32, and support for the elements found in line 5 of the body of the claim is found on page 1, lines 6-7, and page 4 lines 3-5 and lines 7-9.

With respect to claim 22, support for the elements in line 1 of the body of the claim is found on page 4, lines 22-23 and page 5 lines 24-26, support for the elements in lines 2 and 3 of the body is found on page 1, lines 5-6, page 4, lines 3-5, and page 26, lines 31-32, support for the elements in lines 4-5 of the body of the claim is found on page 11 ,lines 6-25, and page 27 lines 8-10, and support for the elements in line 6 of the body of the claim is found on page 1, lines 6-7, page 4, lines 3-5, and page 4, lines 24-26.

6. *Grounds of Rejection To Be Reviewed On Appeal*

Whether claims 1-8, 13-19, 20, and 22-28 are anticipated by *Kermani.*, U.S. Patent No. 6,163,831 under 35 U.S.C. §102(e).

Whether claims 9 and 10 are anticipated by *Kermani.*, U.S. Patent No. 6,163,831 under 35 U.S.C. §102(e).

Whether claims 11, 20, and 30 are anticipated by *Kermani.*, U.S. Patent No. 6,163,831 under 35 U.S.C. §102(e).

Whether claims 12, 21, and 31 are anticipated by *Kermani.*, U.S. Patent No. 6,163,831 under 35 U.S.C. §102(e).

7. *ARGUMENT*

I. Rejection of Claims 1-8, 13-19, 20, and 22-28 under 35 U.S.C. §102(e).

In the Official Action of October 21, 2005, the Examiner rejected claims 1-8, 13-19, 20, and 22-28 under 35 U.S.C. §102(e) as being unpatentable over *Kermani*, U.S. Patent No. 6,163,831. Under the law of anticipation, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP §2131. citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628,

631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

The *Kermani* patent ('831) utilizes hardware elements for controlling access to shared synchronous memory. *Kermani* used a pre-arbiter (920) to direct access to shared synchronous memory by multiple agents (100), (104), (106), and (108). Each of the agents can only access the shared synchronous memory under the control of the pre-arbiter (920) and a switch. *See* Abstract. The pre-arbiter has direct access to the shared synchronous memory. "A requesting agent presents a memory access request and a locking access request to the pre-arbiter (920) and then waits until the current owning agent experiences a lapse of, e.g., one clock cycle in its consecutive memory access. In that case, the locking agent disqualifies the current owning agent of the shared memory from its ownership at the point of lapse and itself assumes ownership of the shared memory." Col. 11, lines 56-63.

However, the processors or agents of *Kermani* are not organized in a hierarchy as claimed by Applicants. The agents or processors of *Kermani* are equally placed in a structure with each agent sharing access to synchronous memory. Each of the agents may submit a memory access request wherein "a winning agent is preferably selected on a priority level assigned to each of the requesting agents." Col. 4, lines 50-52. "Preferably, a unique priority level is established for each of the plurality of agents 100 to 108 either before operation of the system or on-the-fly as the system is operated." Col. 4, lines 52-55. Clearly, *Kermani* assigns a priority to each of the agents in a system. The term "priority" is defined as "superiority in rank, position, or privilege." See Exhibit A attached to Response to Office Action Submitted December 21, 2005. A priority may be assigned within a hierarchical structure, however, the use of a hierarchical structure does not necessitate the assignment of a priority to any element within the hierarchical structure. The following diagram is an example of the position of the agents of *Kermani* with respect to their assigned priorities. As shown, there is no grouping of agents in *Kermani* at an assigned priority level since *Kermani* assigns a unique priority level for each of the agents. See Col. 4, lines 53-54.

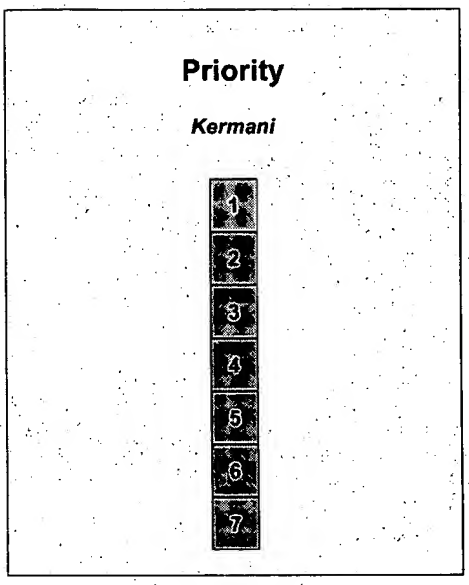


Figure 2: Depiction of priority ranking of seven processors in a system according to the invention of *Kermani*..

In contrast to assignment of priorities, the term hierarchy is defined as "an organizational technique in which items are layered or grouped to reduce complexity." See Exhibit A attached to Response to Office Action Submitted July 21, 2004. The following diagram is an inverted tree structure as an example of a hierarchy, in which a plurality of items are grouped in the layering.

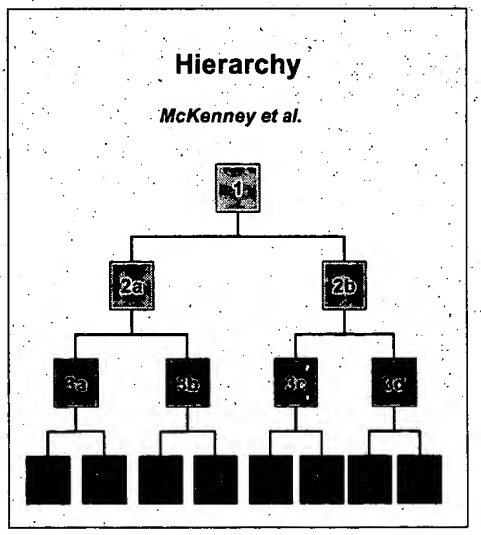


Figure 1: Depiction of hierarchy ranking of fifteen processors in a system according to Applicants' invention.

By definition, and illustration, assignment of a unique priority to each processor in a system is not equivalent to organizing the processors of a system into a hierarchy. A hierarchical structure does not necessitate the assignment of priorities to the elements within that structure, and at the same time provides for a grouping of items, *i.e.* processors, as a set position within the hierarchy. Conversely, a priority is an ordering of elements that does not necessitate the creation of a hierarchical structure. There is no provision in the system of *Kermani* for grouping agents at an assigned priority level since each agent is assigned a unique priority. By definition, such an ordering is required in order to have a hierarchical system. As such, the priority structure of *Kermani* does not provide for a structure in which items are layered or grouped, as in the hierarchy of Applicants.

As noted in the language of Applicants' claims 1, 13, and 22, the processors are organized into a hierarchy and a lock is processed responsive to the hierarchy. It is the placement of the processor requesting the lock in view of the hierarchical organization of the processors of Applicants that is determinative of the order of the processing of the lock among all of the processors in the hierarchy. Conversely, the lock of *Kermani* is responsive to a priority level assigned to a requesting agent. See Col. 4, lines 51-52. There is no provision in *Kermani* to process a lock responsive to a hierarchy, especially since *Kermani* does not organize its agents in a hierarchy. In fact, *Kermani* uses a vertical arrangement of agents with a single agent assigned to each priority level, and grants a lock to an agent based upon an assigned priority level to that agent, if any. This is not processing a lock responsive to a hierarchical structure, it is processing a lock responsive to a ranking within a linear arrangement that only provides for the priority of a single agent in relation to another single agent. The locks of *Kermani* are not responsive to a hierarchy of processors, as the injection of such a hierarchical system in *Kermani* would in fact contradict *Kermani's* own stated system of assigning priorities to agents and assigning locks to agents based upon a priority level. Accordingly, Applicants respectfully contends that the teachings of *Kermani* does not meet the standard set by the CAFC's interpretation of 35 U.S.C. §102(b), and respectfully requests the Board of Patent Appeals rule in Applicants' favor and direct allowance of claims 1-8, 13-19, 20, and 22-28.

II. Rejection of Claims 9 and 10 under 35 U.S.C. §102(e).

In the Official Action of October 21, 2005, the Examiner rejected claims 9 and 10 under 35 U.S.C. §102(e) as being unpatentable over *Kermani*, U.S. Patent No. 6,163,831.

Applicants' remarks with respect to the *Kermani* '831 patent above are hereby incorporated by reference.

Applicants' claim 9 pertains to a data structure within the hierarchy of processors and how this data structure is used to indicate which processors of a group are waiting for a lock. Similarly, Applicants' claim 10 pertains to a data structure within the hierarchy of processors and how this data structure is used to indicate which groups of processors have processors waiting for a lock. In order for *Kermani* to anticipate Applicants' claims 9 and 10, *Kermani* needs to expressly or inherently teach a data structure within the hierarchy for providing the support as claimed by Applicants. Aside from the argument as to whether *Kermani* teaches a hierarchy of processors and processes a lock responsive to the hierarchy, in studying the *Kermani* '831 patent in detail there is not a single provision for the terms data structure or bit mask. With respect to claim 9, the Examiner cited Col. 8, lines 16-24, and with respect to claim 10, the Examiner cited Col. 8, lines 1-15. See Official Action dated October 21, 2005, page 3. Under the law of anticipation, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP §2131 citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

The *Kermani* patent that is being applied by the Examiner for rejecting claims 9 and 10 shows a multiple agent CPU system and sharing access to synchronous memory by the agents. More specifically, the invention of *Kermani* shows a super agent having access to synchronous memory in a clock cycle in which a non-super agent is requesting access to the synchronous memory. It is clearly shown that the non-super agent is not provided access to the synchronous memory during the clock cycle that the super agent has the access, and that the non-super agent

repeats the memory access request in a next clock cycle and repeats the access request in future clock cycles until the super agent has released its access on the synchronous memory. The invention of *Kermani* shows multiple agents requesting access to synchronous memory during adjacent clock cycles. *Kermani* does not show "a data structure having a bit mask indicating which processor of a group are waiting for the lock" nor "a data structure having a bit mask indicating which groups of processors have processors waiting for the lock". There is not one provision within *Kermani* for a data structure or a bit mask, independently or combined. It appears that *Kermani* allows the waiting agent to wait for the next clock cycle to determine if a lapse in the lock acquisition by a prior holding agent exists, to enable a waiting agent to access synchronous memory. Therefore, there is no need for a data structure to monitor processors waiting for a lock in the invention of *Kermani*. As such, there is no inherent need for a data structure in the invention of *Kermani*. Since each and every element as set forth in Applicants' claims 9 and 10 is not either expressly or inherently described in *Kermani*, Applicants respectfully contends that the teachings of *Kermani* does not meet the standard set by the CAFC's interpretation of 35 U.S.C. §102(e), and respectfully requests the Board of Patent Appeals rule in Applicants' favor and direct allowance of claims 9 and 10.

III. Rejection of Claims 11, 20, and 30 under 35 U.S.C. §102(e).

In the Official Action of October 21, 2005, the Examiner rejected claims 11, 20, and 30 under 35 U.S.C. §102(e) as being unpatentable over *Kermani*, U.S. Patent No. 6,163,831.

Applicants' remarks with respect to the *Kermani* '831 patent above are hereby incorporated by reference.

Applicants' claims 11, 20, and 30 pertain to a release flag used by a processor upon release of a lock. Since there is no strict assignment of priorities to Applicants' processors as taught in *Kermani*, the release flag is a tool to facilitate races between processors in between acquisition and release of a lock by a processor. In order for *Kermani* to anticipate Applicants' claims 11, 20, and 30, *Kermani* needs to expressly or inherently teach the limitations present in

these claims. Aside from the argument as to whether *Kermani* teaches a hierarchy of processors and processes a lock responsive to the hierarchy, in studying the *Kermani* '831 patent in detail there is not a single provision for a flag or an equivalent tool for prevent races between acquisition and release of the lock. Since *Kermani* assigns priorities to each of its agents, *Kermani* dose not have any need for a release flag. Each agent in *Kermani* has a unique assigned priority and the lock is processed in response to this unique priority. With further respect to claims 11, 20, and 30, the Examiner cited Col. 6, lines 17-30. *See* Official Action dated October 21, 2005, page 4. This specific cite discusses providing access to shared memory by one of the sub-ordinate agents during an "open window" period. However, there is no express or inherent teaching in this section of *Kermani*, or any other section of *Kermani*, for use of a release flag to facilitate races between processors. As stated above, based upon the assigned priorities of *Kermani*, there is no inherent need for such a flag. Under the law of anticipation, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP §2131. citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). However, *Kermani* neither expressly or inherently describe a release flag in the manner as claimed by Applicants, nor requires a release flag in order to function within its intended structure.

Since each and every element as set forth in claims 11, 20, and 30 is not either expressly or inherently described in *Kermani*, Applicants respectfully contends that the teachings of *Kermani* does not meet the standard set by the CAFC's interpretation of 35 U.S.C. §102(e), and respectfully requests the Board of Patent Appeals rule in Applicants' favour and direct allowance of claims 11, 20, and 30.

IV. Rejection of Claims 12, 21, and 31 under 35 U.S.C. §102(e).

In the Official Action of October 21, 2005, the Examiner rejected claims 12, 21, and 31 under 35 U.S.C. §102(e) as being unpatentable over *Kermani*, U.S. Patent No. 6,163,831.

Applicants' remarks with respect to the *Kermani* '831 patent above are hereby incorporated by reference.

Applicants' claims 12, 21, and 31 pertain to a handoff flag associated with grant of a lock from a group of processors in possession of a lock to a processor requesting an unconditional lock. In order for *Kermani* to anticipate Applicants' claims 12, 21, and 31, *Kermani* needs to expressly or inherently teach the limitations present in these claims. Aside from the prior argument as to whether *Kermani* teaches a hierarchy of processors and processes a lock responsive to the hierarchy, in studying the *Kermani* '831 patent in detail there is not a single provision for a lock to be grants from one processor or group of processors to another processor or group of processors. With respect to claims 12, 21, and 31, the Examiner cited Col. 6, lines 5-16. *See* Official Action dated October 21, 2005, page 4. This specific cite discusses "rules with respect to access provided to the shared synchronous memory". Col. 6, lines 5-6. Aside from the pre-emptive property of the super-agent, the rules are not specific. They merely indicate that non-super agents may arbitrate for access to the shared synchronous memory, such as "on a first come first served basis, on a priority basis, or other suitable decisive criteria . . ." Col. 6, lines 13-15. Under the law of anticipation, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP §2131. citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). However, *Kermani* does not expressly or inherently describe a handoff flag in the manner as claimed by Applicants. Applicants' handoff flag is transferred among processors or groups of processors associated with conditional and unconditional locks.

The *Kermani* patent that is being applied by the Examiner for rejecting claims 12, 21, and 31 shows an arbiter-and- switch, *i.e.* a hardware element, that determines access to shared synchronous memory. There is no express or inherent description for a handoff flag associated with the transfer or grant of a lock from a group of processors. Rather, in *Kermani* it is the arbiter-and-switch that determines grant and handoff of a lock. Similarly, there no express or inherent description in *Kermani* for differentiating between a conditional and an unconditional

lock associated with the handoff flag. In fact, *Kermani* discloses a "lock" and does not distinguish between conditional locks and unconditional locks, as claimed by Applicants. The arbiter-and-switch of *Kermani* monitors access to the shared synchronous memory and determines access windows for agents that submit requests. The arbiter-and-switch of *Kermani* grants a lock, and does not provide an express or inherent teaching of a conditional or unconditional lock. Since each and every element as set forth in claims 12, 21, and 31 is not either expressly or inherently described in *Kermani*, Applicants respectfully contends that the teachings of *Kermani* does not meet the standard set by the CAFC's interpretation of 35 U.S.C. §102(e), and respectfully requests the Board of Patent Appeals rule in Applicants' favour and direct allowance of claims 12, 21, and 31.

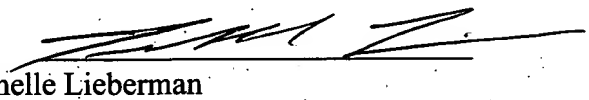
IV. Conclusion

In view of the rejections presented by the Examiner in the Office Action made final, it appears clear on the record that the *Kermani* patent do not anticipate Applicants' invention based upon the legal definition of obviousness. Although the prior art patent cited by the Examiner relates to a computer system having shared synchronous memory and a hardware element for controlling access to the shared memory, the placement of the processors and the tools used to control access to the shared memory of *Kermani* are different than that claimed by Applicants.

Applicants believe that those skilled in the art have failed to solve the problem as claimed

by Applicants. Accordingly, for the reasons outlined above, Applicants respectfully requests the Board of Patent Appeals direct allowance of this application and all pending claims.

Respectfully submitted,

By: 
Rochelle Lieberman
Registration No. 39,276
Attorney for Applicants

Lieberman & Brandsdorfer, LLC
802 Still Creek Lane
Gaithersburg, MD 20878
Phone: (301) 948-7775
Fax: (301) 948-7774
email: rocky@legalplanner.com

Date: March 23, 2006

8. Claim Appendix:

1. A method for efficiently handling high contention locking in a multiprocessor computer system, comprising:

organizing at least some of the processors into a hierarchy;

providing a lock selected from the group consisting of: an interruptible lock, and a lock which waits using only local memory; and

processing the lock responsive to the hierarchy.

2. The method of claim 1, wherein the processing step conditionally acquires the lock.

3. The method of claim 1, wherein the processing step returns a failure to grant the lock if the lock is not immediately available.

4. The method of claim 1, wherein the processing step unconditionally acquires the lock.

5. The method of claim 4, wherein the processing step spins on the lock until the lock is available.

6. The method of claim 4, further comprising allowing system interrupts while spinning on the lock

7. The method of claim 1, wherein the processing step unconditionally releases the lock.

8. The method of claim 1, wherein the processing step the processors spin on private memory.

9. The method of claim 1, wherein the hierarchy includes a data structure having a bit mask indicating which processors of a group are waiting for the lock.

10. The method of claim 1, wherein the hierarchy includes a data structure having a bit mask indicating which groups of processors have processors waiting for the lock.

11. The method of claim 1, further comprising maintaining a release flag for a group of processors to prevent races between acquisition and release of the lock.

12. The method of claim 1, further comprising maintaining a handoff flag for a group of processors to grant the lock to a processor requesting an unconditional lock from a processor requesting a conditional lock.

13. A computer system comprising:

multiple processors;

a lock selected from the group consisting of: an interruptible lock, and a lock which waits using only local memory; and

a hierarchical representation of processor organization; and

a lock primitive for processing the lock responsive to the hierarchy.

14. The computer system of claim 13, wherein said primitive further comprises a conditional lock acquisition primitive.

15. The computer system of claim 14, wherein said conditional lock acquisition further indicates a lock failure if said lock is not immediately available.

16. The computer system of claim 13, wherein said primitive further comprises an unconditional lock acquisition primitive.

17. The computer system of claim 16, wherein said processor may enter a spin stage of said lock is not immediately available.

18. The computer system of claim 16, wherein said lock may be subject to a system interrupt during a spin stage.

19. The computer system of claim 13, wherein said primitive further comprises a primitive for an unconditional release of said lock.

20. The computer system of claim 13, wherein said primitive further comprises a release flag to prevent races between acquisition and release of the lock.

21. The computer system of claim 13, wherein said primitive further comprises a handoff flag to grant a lock to a processor requesting an unconditional lock from a processor requesting a conditional lock.

22. An article comprising:

a computer-readable signal bearing medium; multiple processors;

means in the medium for hierarchically organizing at least some of the processors of a computer system;

means in the medium for providing a lock selected from the group consisting of: an interruptible lock, and a lock which waits using only local memory; and

means in the medium for processing the lock responsive to the hierarchy.

23. The article of claim 22, wherein the medium is a recordable data storage medium.

24. The article of claim 22, wherein the medium is a modulated carrier signal.

25. The article of claim 22, wherein the means is a conditional lock acquisition primitive.

26. The article of claim 25, wherein a lock failure is indicated if the lock is not immediately available.

27. The article of claim 22, wherein the means is an unconditional lock acquisition

primitive.

28. The article of claim 28, wherein a .spin stage is entered by a processor if the lock is not immediately available.

29. The article of claim 22, wherein the means is an unconditional lock release primitive.

30. The article of claim 22, wherein said means is a release flag responsive to races between acquisition and release of a lock.

31. The article of claim 22, wherein said means is a handoff flag responsive to a processor requesting an unconditional lock from a processor requesting a conditional lock.

9. Evidence Appendix

MPEP §2131

U.S. Patent No. 6,163,831 to *Kermani*

10. Related Proceedings Appendix:

None

Go to **MPEP - Table of Contents**

browse before

2131 Anticipation - Application of - 2100 Patentability

2131 Anticipation - Application of 35 U.S.C. 102(a), (b), and (e) [R-1]

35 U.S.C. 102 Conditions for patentability; novelty and loss of right to patent.

A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent, or

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States, or

(c) he has abandoned the invention, or

(d) the invention was first patented or caused to be patented, or was the subject of an inventor's certificate, by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application for patent or inventor"s certificate filed more than twelve months before the filing of the application in the United States, or

**>

(e) the invention was described in - (1) an application for patent, published under **section 122(b)**, by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in **section 351(a)** shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under **Article 21(2)** of such treaty in the English language; or<

(f) he did not himself invent the subject matter sought to be patented, or

(g)(1) during the course of an interference conducted under **section 135** or **section**

291, another inventor involved therein establishes, to the extent permitted in **section 104**, that before such person's invention thereof the invention was made by such other inventor and not abandoned, suppressed, or concealed, or (2) before such person's invention thereof, the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it. In determining priority of invention under this subsection, there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). >"When a claim covers several structures or compositions, either generically or as alternatives, the claim is deemed anticipated if any of the structures or compositions within the scope of the claim is known in the prior art." *Brown v. 3M*, 265 F.3d 1349, 1351, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) (claim to a system for setting a computer clock to an offset time to address the Year 2000 (Y2K) problem, applicable to records with year date data in "at least one of two-digit, three-digit, or four-digit" representations, was held anticipated by a system that offsets year dates in only two-digit formats). See also MPEP § **2131.02**.< "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Note that, in some circumstances, it is permissible to use multiple references in a **35 U.S.C. 102** rejection. See **MPEP § 2131.01**.

browse after

03-24-06

AF
IFW

PATENT
Attorney Docket No.: BEA9-2000-0013-US1

BOARD OF PATENT APPEALS
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	McKenney et al.		
SERIAL NO.:	09/753,062	Group Art Unit:	2112
FILING DATE:	December 28, 2000	Examiner:	Huynh, K.
FOR:	**Quad Aware Locking Primitive**		

TRANSMITTAL LETTER

Mail Stop: Appeal Brief - Patent
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

EXPRESS MAIL CERTIFICATE
Express Mail Label No.: ED 941833224 US
Date: March 23, 2006

I hereby certify that I am depositing the enclosed or attached paper with the U.S. Postal Service "Express Mail Post Office to Addressee" service on the above date, addressed to Mail Stop Appeal Brief - Patent, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Rochelle Lieberman, Reg. No. 39,276

Sir:

Enclosed is a Brief in Support of Appeal with copies of all references which were relied upon by Appellant, and a Credit Card Payment Form in the amount of $500.00 pursuant to 37 C.F.R. §1.17(c).

Respectfully submitted,

By:
Rochelle Lieberman, Esq.
Registration No. 39,276
Attorney for Applicant

Lieberman & Brandsdorfer, LLC
802 Still Creek Lane
Gaithersburg, MD 20878
Phone: (301) 948-7775
Fax: (301) 948-7774
email: rocky@legalplanner.com
Date: March 23, 2006